Temperature compensation of piezoresistive pressure sensors

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Abstract

A major problem associated with piezoresistive pressure sensors is their cross sensitivity to temperature. The influence of temperature is manifested as a change in the span and offset of the sensor output. Moreover, in batch fabrication, minor process variations change the temperature characteristics for individual units. In this paper, a simulation model for the batch fabrication of piezoresistive pressure sensors is presented. An error band for the sensor response is determined in terms of processing variations for a temperature range of −40 to 130 °C over a pressure range of 0 to 45 psi. Utilizing this information, a new temperature-compensation technique, especially suited for batch fabrication, is described. This technique shows very encouraging results in removing the zero pressure offset and significantly reduces the errors caused by processing variations on the same wafer.

1. Introduction

Ongoing advances in IC fabrication, micromachining, and packaging technologies have sparked a new phase of development for silicon-based integrated smart pressure sensors. It is interesting to note that for many smart sensors, the performance of the overall device depends more on the interface electronics than on the transduction element. Additionally, an important factor for the economic success of smart sensors is the use of batch-fabrication techniques to bring down the cost of individual units.

A particular sensor of current interest is the piezoresistive pressure sensor where a thin diaphragm is etched from the substrate. Piezoresistors, whose resistivity is dependent on the strain developed in the diaphragm, are formed on top of the diaphragm. The piezoresistors are most often connected in a bridge circuit to increase the sensitivity and decrease cross sensitivity. A major problem associated with piezoresistive pressure sensors, however, is the inherent cross sensitivity to temperature. The influence of temperature on a piezoresistive pressure sensor is exhibited by a change in the span and offset of the sensor output. Moreover, minor process variations give rise to piezoresistive tracking errors, which in turn change the temperature characteristics for individual units. Temperature-compensation techniques have

been reported using laser trimming, external resistors, and clever use of material properties [1–3]. Generally these techniques are for limited temperature and pressure ranges, and in many cases for specific applications such as biomedical devices. Moreover, these techniques involve additional processing steps performed under sensor operating conditions, which add time and cost to the device fabrication process.

Until recently the design of circuits to compensate for temperature cross sensitivity has been intuitive, as few detailed design aids exist. Some effort, however, has gone into the simulation of piezoresistive pressure sensors [4–6]. These simulation techniques provide a means to study the effect of various cross-sensitivity parameters, providing information to be used in compensation and interface circuit design without an in-depth detailed analysis of the physics and mechanics of the sensor structure. Progress in this area is important, as it will ultimately lead to more effective computer-aided design (CAD) of integrated sensors.

In this paper, the results of simulation studies and temperature compensation for piezoresitive pressure sensors are presented. A sensor model, developed from the viewpoint of evaluating the sensor I/O characteristics as a function of pressure and temperature, is presented. Simulation results for three piezoresistive layouts are presented in Section 3. Based on these results, a piezoresistor

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layout exhibiting the highest pressure sensitivity and least nonlinearity is selected. This structure is studied further in Section 4 for piezoresistive tracking errors, and the sensor model is enhanced to include the effects of batch fabrication. Simulation results to evaluate sensor performance as a function of pressure, temperature, and tracking errors are presented and discussed in Section 5. Based on these results, a new temperature-compensation technique and its results are presented in Section 6. Finally, a discussion of the work completed is contained in Section 7.

2. Sensor model

The characteristics of a piezoresistive pressure sensor are determined by its structure; similar structures produce similar results. A realistic sensor structure will be analyzed here from the viewpoint of evaluating the temperature and pressure characteristics of the sensor. The results of this analysis can easily be extended to other similar structures. In this Section various parameters of the sensor model will be determined. A sensor simulation program that requires a low-level physical model is used for the evaluation of the temperature and pressure characteristics of the sensor [4]. The sensor analyzed here is composed of three layers: the thin silicon diaphragm, a 1 μm thick layer of silicon dioxide grown over the diaphragm at 850 °C, and the package (Corning glass support plate) sealed at 450 °C with a hole for the applied pressure. The piezoresistors are diffused in a Wheatstone bridge configuration on the thin silicon diaphragm. The sensor structure and its corresponding electrical circuit are shown in Fig. 1. The four resistors are nominally equal in value and arranged such that the parallel resistors (RP) increase while the transverse resistors (RT) decrease with the application of pressure (strain). The deflection of the diaphragm is assumed to be small compared to its thickness. Under these conditions, a first-order approximation of the sensor output for $\Delta R \ll R$ is given by

$$V_o = V_{cc} \frac{\Delta R}{R}$$

The diaphragm thickness determines the pressure sensitivity. The stresses in the thin silicon diaphragm caused by an applied pressure are inversely pro-
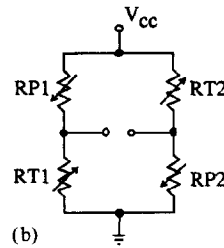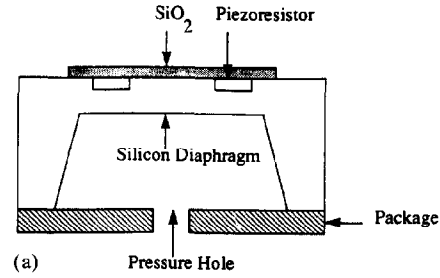

Fig. 1. Piezoresistive pressure sensor: (a) sensor structure; (b) electrical circuit.

portional to the square of the diaphragm thickness. The effect of process-induced thickness variation can be made smaller by increasing the nominal thickness, but this can be done only at the cost of pressure sensitivity. The size of the diaphragm also affects the pressure sensitivity. A larger diaphragm is more sensitive and the stress increases from the center to the diaphragm edge. Therefore, a piezoresistor placed close to the edge is more sensitive, but its sensitivity is more vulnerable to process variations in diaphragm size, alignment, and piezoresistor location. Based on these considerations, the example diaphragm is assumed to be square with a side length of 1000 μm and a uniform thickness of 10 μm. All piezoresistors are placed 20 μm from the diaphragm edge.

There is also a tradeoff between pressure sensitivity and reproducibility for piezoresistors. Specifically, an increase in resistor size improves the device reproducibility but decreases the sensitivity because of the stress-averaging effect. A smaller size (width) also implies increased tracking errors. A decrease in resistor width from 15 to 5 μm results in an increase of design tolerance from ±20 to ±40% [7]. The piezoresistor width for our example model has been set to 10 μm to strike a balance. The sheet resistance is chosen to be 200 Ω/square with a junction depth of 2.7 μm. This

is a good compromise for producing resistors, since the sheet resistance is convenient and the tolerances and temperature ceofficients are acceptable [7]. Typical measured sheet resistance values plotted in ref. 7 show that the temperature coefficient for a 200 Ω/square value is fairly linear. Moreover, these are typical values for the base diffusion and will save a diffusion step if bipolar function transistors are included elsewhere in the circuit. The piezoresistor values obtained for our dimensions are 2 kΩ. Piezoresistor values in the range 500 to 5000 Ω have been reported by manufacturers and in the literature [8–10].

3. Piezoresistor layouts

Various piezoresistor layouts on a diaphragm are possible. Moreover, pressure sensitivity and linearity are a function of the piezoresistor locations. As an initial step, a number of layouts with differing locations and arrangements, some gleaned from previous work [4, 10], were evaluated using the simulator described in ref. 4. Three of these layouts were modeled and evaluated further. These layouts are shown in Fig. 2. Cartesian coordinates, using the diaphragm center as the origin for the piezoresistor center, are shown in the Figure. RP and RT denote parallel and transverse resistors, respectively. Some of the characteristics of the layout models are summarized in Table 1.

Layout 1 has two parallel and two transverse piezoresistors. Each resistor is 100 μm long and 10 μm wide. The resistors are placed near the four edges of the diaphragm. This layout provides a pressure sensitivity of 33.25 mV/psi. The second

TABLE 1. Characteristics of various piezoresistor layouts

Characteristic	Layout 1	Layout 2	Layout 3
Pressure sensitivity (mV/psi)	33.25	35.65	31.62
% Nonlinearity	1.023	0.242	−0.419
Temperature coefficient of pressure sensitivity (μV/psi °C)	78.66	81.98	70.94

layout provides an improvement over the first one. In this case the transverse resistors were broken into two identical legs to increase the average stress over the piezoresistors. Now each transverse resistor is 50 μm long but with the same width of 10 μm. This increases the sensitivity to 35.65 mV/ psi. A third layout places all resistors close together and near one diaphragm edge to reduce the tracking errors. In this third case, the piezoresistors are broken into two parts to improve the average stress over them. The pressure sensitivity for this layout is 31.62 mV/psi.

Pressure sensitivity as a function of temperature is plotted in Fig. 3. Layout 2 has the highest pressure sensitivity. For all three layouts the pressure sensitivity decreases with temperature because the temperature coefficient of piezoresistivity is negative.

Figure 4 shows the output voltage for the three layouts for applied pressures of 15 and 45 psi. The percentage nonlinearity computed using end points for the three layouts is included in Table 1. Again, layout 2 produces the maximum output with the least nonlinearity. The zero pressure offset for all three layouts is nil, since the bridge is composed of matching resistors. Moreover, the
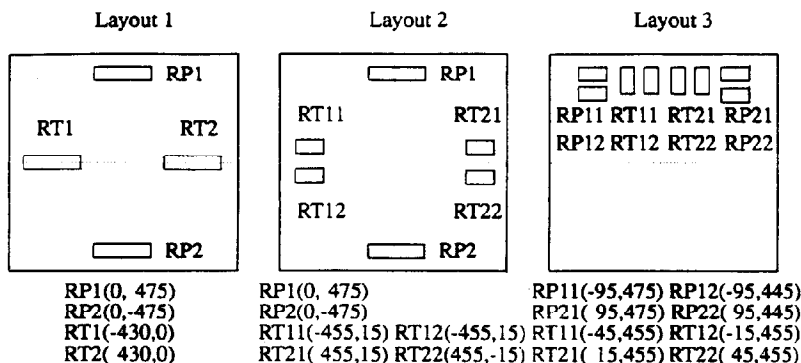

Fig. 2. Piezoresistor layouts on a diaphragm and their Cartesian coordinates in micrometers (not to scale).
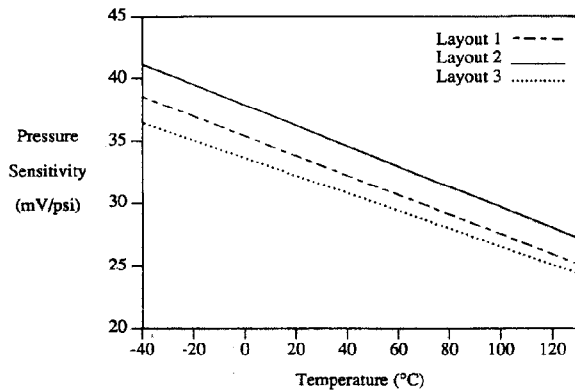
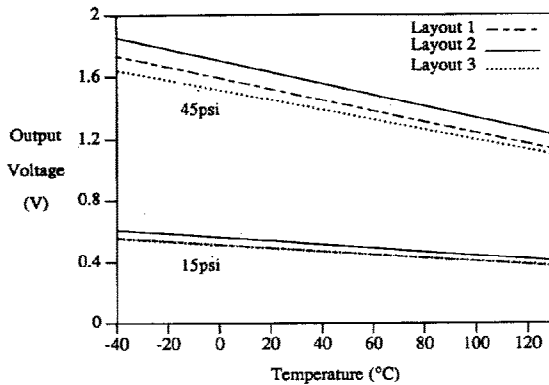Fig. 3. Pressure sensitivity for the three layouts.

Fig. 4. Output voltage for the three layouts.

offset remains zero over the entire temperature range because temperature changes for individual piezoresistors are cancelled due to the bridge structures.

4. Tracking errors

Based on the results of Section 3, layout 2 is chosen for further analysis. In this Section a model will be developed from the viewpoint of batch fabrication of the piezoresistive pressure sensors. As discussed earlier, batch fabrication gives rise to tracking errors. Tracking errors are caused by variations in temperature, time period, impurity concentration, mask alignment, and other environmental changes seen by different silicon wafers processed in a batch. There is no cost-effective technique for monitoring resistance while the diffusion is taking place; in fact, at the temperatures used, silicon is no longer a semiconductor.

Thus the effect of diffusion can be measured only after the wafer has been cooled, when a subsequent correction is difficult and expensive. The end result is a variation in resistance values. These variations need to be modeled and handled in two different ways: wafer-to-wafer variations and variations on the same wafer.

Wafer-to-wafer variations are large compared to the variations seen on the same wafer. Variations of 10 to 25% from the nominal values have been reported for different wafers [7]. Variations on the same wafer are caused by temperature gradients, uneven flow of dopant gas within the furnace, shape and size of resistors, and mask inaccuracy. Variations on the order of 1 to 3% have been reported for 10 μm wide resistors [7].

To model the two types of tracking errors rather large figures of ±20 and ±2.5% were chosen for wafer-to-wafer and same-wafer variations, respectively. Simulations were run by introducing errors in various possible combinations of four piezoresistors. It was concluded that the worst-case errors in the output voltage are obtained by introducing total error in either the parallel or transverse resistor pair. Thus to represent wafer-to-wafer variations, all the piezoresistors are changed by ±20% of their nominal values. To add the effect of variations on the same wafer, the ±20% wafer-to-wafer variation for transverse resistors was modulated by a ±2.5% variation. Appropriate changes were also made in the sheet resistance and the temperature coefficient of resistivity. Thus the individual units have piezoresistor values within ±2.5%, whereas values for the batch fall within ±22.5% of the nominal values.

5. Results

Using the model described in Sections 2 and 4, a large number of simulations generated the sensor performance data for a broad pressure and temperature range as a function of tracking errors. The data provide a worst-case error band for various characteristics of the batch-fabricated piezoresistive pressure sensors. It was seen that all sensor parameters are functions of temperature and tracking errors.

The error bands for pressure sensitivity are shown in Fig. 5. The narrow bands result from the tracking variations on the same wafer. At
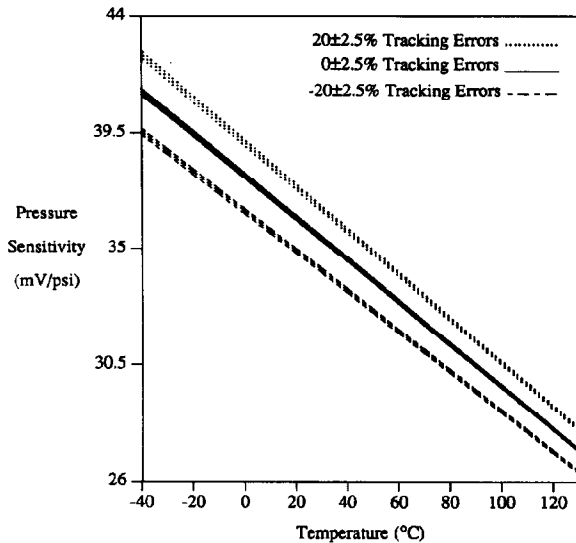
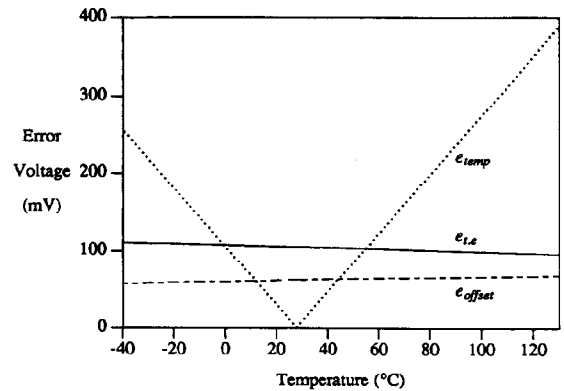Fig. 5. Pressure sensitivity for various tracking errors.

Fig. 6. Error voltages for the sensor.

The errors caused by tracking errors and temperature can be subdivided into three parts:

$$e_{\text{Total}} = e_{\text{offset}} + e_{\text{t.e.}} + e_{\text{temp}}$$

where e_{offset} is the zero pressure offset voltage, mainly caused by on-chip tracking errors that cause an imbalance in the piezoresistive bridge. The offset error is also a function of temperature. $e_{\text{t.e.}}$ is the error caused by wafer-to-wafer and same-wafer tracking errors. These errors only shift the sensor response curve as a function of the magnitude of the tracking errors. e_{temp} are the errors solely due to the temperature, since the piezoresistivity is a function of temperature [11]. These errors are present even in a sensor with perfectly matched piezoresistors. The good thing about the temperature dependency is that the relation is linear, at least to a first-order approximation. The magnitude of these errors as a function of temperature is shown in Fig. 6 for a sensor with positive tracking errors. The polarity of the error voltages is different for various tracking-error patterns. Room temperature is taken as reference for the e_{temp} error plot. Thus, the error is zero at 27 °C and increases linearly on either side.

6. Double bridge temperature-compensation technique

Based on the results of Sections 4 and 5, a new temperature-compensation technique using two bridges is proposed. The block diagram of this technique is shown in Fig. 7. A piezoresistive bridge is located on the thin diaphragm and its output is a function of pressure and temperature.

room temperature a maximum variation of 0.105 mV/psi is observed for an individual unit. The wider band extending from 39.45 mV/psi to 42.60 mV/psi at −40 °C indicates the error band for the whole batch. At room temperature a maximum variation of 1.35 mV/psi is observed for the batch. It is also observed that a higher pressure sensitivity is obtained with larger bridge resistance values and for the units with −2.5% tracking errors. The pressure sensitivity is a function of temperature even for the sensor with the perfectly matched piezoresistors, although the variation is linear. For the structure with no tracking errors of any type, the pressure sensitivity decreases from 41.13 to 27.20 mV/psi as the temperature rises from −40 to 130°C. The error band is much smaller for on-chip variations compared to the wafer-to-wafer variations, and is wider for lower temperatures.

An additional component of error voltage is introduced by the zero pressure offset, which is mainly caused by the tracking errors. Offset values of 56.8 to 68.7 mV are observed for ±2.5% tracking errors for the temperature range −40 to 130 °C. The temperature dependency of the zero pressure offset also shows a nonlinearity of 1.30% for positive tracking errors and 1.26% for negative tracking errors. The offset voltages for positive and negative tracking errors are almost of the same magnitude.
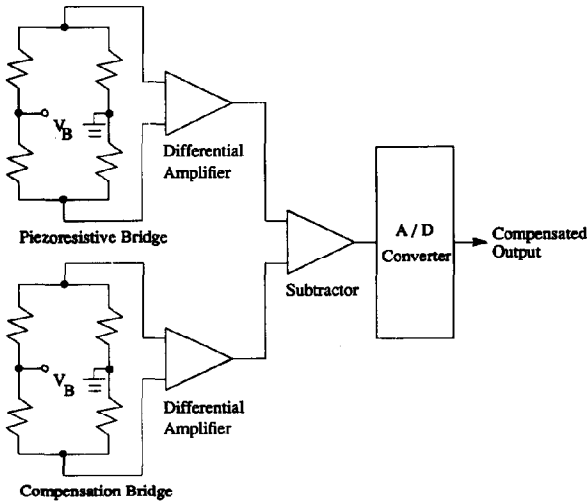
Fig. 7. Block diagram of the double bridge temperature-compensation technique.

The compensation bridge is located on the bulk part of the chip; thus its response is dependent on the temperature only. The shape and size of compensation bridge resistors are identical to the corresponding resistors of the pressure-sensitive bridge. Physically the corresponding arms of the two bridges are located as close as possible to each other. To prevent the effects of induced stress in the diaphragm, a safe distance of 100 µm from the diaphragm edge has been suggested for the peripheral circuits [10]. These physical considerations and the close proximity of the resistors eliminate the factors contributing to tracking errors on the same chip, thus the variations between the corresponding bridge arms are negligible [7]. Therefore the effect of same-wafer tracking errors can be eliminated by taking the difference of the two bridge outputs. Differential amplifiers are used to amplify and convert the double-ended bridge output to a single-ended signal. An analog subtracter circuit is used to generate the difference of the two bridge outputs. The use of the subtractor eliminates the need for two analog-to-digital converters. Moreover, the output of the subtracter is a unipolar signal that doubles the resolution of the analog-to-digital converter. The output of the subtracter is digitized for further processing to produce a temperature-compensated digital output.

To simulate the double bridge technique, rather large figures were chosen to model the tracking errors. The tracking error values are summarized

TABLE 2. Piezoresistor tracking error values

Configuration	Component	Tracking error (%)
Wafer to wafer	Temperature bridge	±20
	Piezoresistive bridge	±20
Same wafer/chip	Temperature bridge	±2.5
	Piezoresistive bridge	±2.5
Same chip	Corresponding bridge arms	Negligible

in Table 2. The simulator of ref. 4 was used to simulate the piezoresistive bridge. The compensation bridge and the analog circuit were simulated with PSpice 4.03 and the digital section of the analog-to-digital converter was simulated with VHDL. Simulations for the double bridge compensation technique for a temperature range −40 to 130 °C show encouraging results for the temperature compensation of the zero pressure offset and the errors caused by the tracking errors on the same chip. Zero pressure offset, which is a function of tracking errors and temperature, shows a maximum nonlinearity of 1.30% with a worst-case error band of ±68 mV over the desired temperature range. It is reduced to a fraction of a microvolt for the compensated sensor, which is below the measurement precision limit. Zero pressure offset curves for the compensated and uncompensated sensors with ±2.5% tracking errors are shown in Fig. 8. The curve in the middle, centered around zero, shows the compensated zero pressure offset for all types of tracking errors. The curves at the top and bottom represent the offset values for positive and negative tracking errors, respectively.

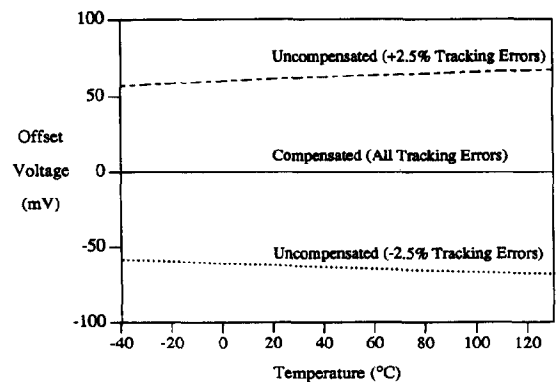The sensor output is also a function of temperature and tracking errors. Sensors with ±2.5%
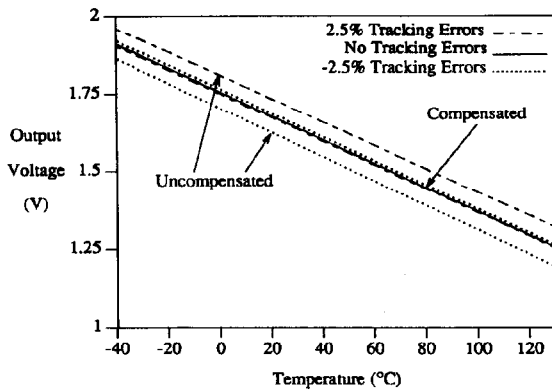

Fig. 8. Compensated zero pressure offset.

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Fig. 9. Compensated output voltage.

tracking errors show a worst-case error band of ±3.04% of the full-scale output for 45 psi. The error band is reduced to ±0.24% of the full-scale output for the compensated sensor. A plot of the sensor response for both cases is shown in Fig. 9.

The double bridge technique eliminates the zero pressure offset and compensates for the output variation caused by the on-chip tracking errors. The technique is not effective for wafer-to-wafer tracking errors and the errors contributed by the temperature dependency of piezoresistance. Work is underway to compensate for these two factors by using additional circuits and digitally processing the output of the analog-to-digital converter.

7. Conclusions

Piezoresistive pressure sensors have been modeled from the viewpoint of batch fabrication. This aspect is very important for the economical development of integrated sensors, since batch fabrication is the kay factor in lowering the costs of these devices. The same model can be used for other integrated sensors making use of diffused piezoresistors.

The sensor performance has been evaluated using this model and a double bridge technique has been suggested for temperature compensation of same-wafer tracking errors. The technique uses a very simple circuit employing diffusion steps only. Most temperature-compensation techniques reported in the literature use laser trimming of resistor networks. These resistor networks use many type of resistors. In many cases diffusion,

ion implantation, and film-deposition techniques have been combined on the same chip. Software techniques have also been reported, but these are considerably slower than the hardware techniques.

The technique presented here covers a wider temperature and pressure range than most techniques reported in the literature. The sensor output error band has been reduced to a maximum of ±0.24% of the full-scale output. The zero pressure offset has been reduced below the measurement precision limit for all types of tracking errors. The output accuracy is comparable to the ones reported in the literature, whereas the zero pressure offset is much better than most published results, which range from ±0.2 to 1% of the full-scale output.

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